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| 09/887,559 | 06/25/2001 | Edward C. Nevill | 550-242 | 7548 |

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| EXAMINER | |
|---|---|
| O BRIEN, BARRY J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2183 | 12 |

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/887,559 | NEVILL ET AL. | |
| | Examiner | Art Unit | |
| | Barry J. O'Brien | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *6/25/01 to 3/31/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6, 7, 11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-17 have been examined.

### *Papers Submitted*

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration as received on 10/16/01, Specification as received on 10/16/01, Priority Papers as received on 10/16/01, IDS as received on 10/16/01, IDS as received on 11/21/01, Pre-Amendment A as received on 6/25/01, Pre-Amendment B as received on 10/31/02, Change of Address as received on 3/31/04 and IDS as received on 3/31/04.

### *Specification*

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

5. The abstract of the disclosure is objected to because of the following informalities:

   a. The abstract contains reference numerals 104 and 108. Because it is an abstract, it is unclear what the reference numerals correspond to. Please remove the reference numerals from the abstract.

b. The abstract contains a line reciting, "[Figure 8]". It is unclear why this phrase is in the abstract, as no figure is present. Please remove the above phrase from the abstract.

Correction is required. See MPEP § 608.01(b).

***Claim Objections***

6. Claim 17 is are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

7. Claims 17 recites the limitation, "A computer program product holding a computer program for controlling a computer to perform the method of claim 16". The parent claim of claim 17, claim 16, already claims the execution of instructions to control processing, instructions that inherently reside on some sort of computer readable medium (computer program product). Therefore, because there is no way that the processing of instructions of claim 16 can function as claimed without the instructions being comprised on a computer program product, claim 17 fails to further limit the subject matter of claim 16.

8. Claims 1-15 are objected to because of the following informalities:

a. Claim 1 recites the limitation, "Apparatus for processing data" in its preamble. Please amend the claim language to read, "An apparatus for processing data" in order to be more grammatically correct. The same correction needs to also be made for dependent claims 2-15.

b. Claim 13 recites the limitation, "said register bank hold stack operands from a top potion of said stack". Please amend the claim language to read, "said register bank holds stack operands from a top portion of said stack" in order to be more grammatically correct.

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 3 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 3 recites the limitation, "said translator output signals include control signals that control operation of said processor core and match signals produced on decoding instructions of said first instruction set". It is unclear whether "match signals" refers to a separate group of signals of the translator output signals simply called "match signals", or if it refers to the "control signals" being equal to signals "produced on decoding instructions of a said first instruction set". Please correct the claim language to more clearly define the metes and bounds of the invention. For the purposes of this examination, the Examiner will assume that "match signals" refer to "control signals" being equal to signals "produced on decoding instruction of a said first instruction set".

12. Claim 11 recites the limitation "second instruction" on its last line. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this examination, the Examiner will assume that this limitation refers to the "said instruction set" claimed in parent claim 1.

### *Claim Rejections - 35 USC § 102*

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1-7, 11-12 and 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Robinson et al., U.S. Patent No. 5,307,504.

15. Regarding claim 1, Robinson has taught an apparatus for processing data, said apparatus comprising:

a. A processor core (20 of Fig.1) operable to execute operations as specified by instructions of a first instruction set (see Col.5 lines 51-55),

b. An instruction translator (40 of Fig.2) operable to translate instructions of a second instruction set into translator output signals corresponding to instructions of said first instruction set (see Col.6 lines 20-43), at least one instruction of said second instruction set specifying an operation to be executed using one or more input variables (see Col.6 lines 52-57),

c. An interrupt handler responsive to an interrupt signal to interrupt execution of operations corresponding to instructions of said first instruction set after completion of execution of a currently executing operation (see Col.7 line 61 – Col.8 line 2),

d. Restart logic for restarting execution after said interrupt (see Col.7 lines 38-60).

e. Wherein said instruction translator is operable to generate a sequence of one or more sets of translator output signals corresponding to instructions of said first instruction set to represent said at least one instruction of said second instruction set (see Col.7 lines 6-37), each sequence being such that no change is made to said one or more input variables until a final operation within said sequence is executed (see Col.11 lines 58-65),

f. After occurrence of an interrupt during execution of a sequence of operations representing said at least one instruction of said second instruction set:

I. If said interrupt occurred prior to starting execution of a final operation in said sequence, then said restart logic restarts execution at a first operation in said sequence (see Col.7 lines 38-60),

II. If said interrupt occurred after starting execution of a final operation in said sequence, then said restart logic restarts execution at a next instruction following said sequence (see Col.7 line 61 – Col.8 line 33).

16. Regarding claim 2, Robinson has taught an apparatus as claimed in claim 1, wherein said translator output signals include signals forming an instruction of said first instruction set (see Col.6 lines 20-27).

17. Regarding claim 3, Robinson has taught an apparatus as claimed in claim 1, wherein said translator output signals include control signals that control operation of said processor core and match control signals produced on decoding instructions of said first instruction set (see Col.6 lines 1-6). Here, the instructions (control signals) are the same for both the directly compiled RISC instructions and the translated CISC-to-RISC Instructions (see Fig.1).

18. Regarding claim 4, Robinson has taught an apparatus as claimed in claim 1, wherein said translator output signals include control signals that control operation of said processor core and specify parameters not specified by control signals produced on decoding instructions of said first instruction set (see Col.7 lines 6-37). Here, the instruction ordering criteria is an output of the X-Y translator to control the processor on how to further group the translated instructions. The ordering criteria are not used for the decoding of instructions already in the Y (native) format (see Fig.1).

19. Regarding claim 5, Robinson has taught an apparatus as claimed in claim 1, wherein said restart logic is part of said instruction translator (see Col.7 line 3 – Col.8 line 33). Here, the method of interrupt handling and restarting of execution following the interrupt is performed within the translation system (40 of Fig.2), and thus the logic to perform the interrupt handling and restarting of execution is inherently within the translation system as well.

20. Regarding claim 6, Robinson has taught an apparatus as claimed in claim 1, wherein said restart logic stores a pointer to a restart location within instructions of said second instruction set that are being translated, said pointer being advanced upon execution of said final operation (see Col.7 lines 38-50).

21. Regarding claim 7, Robinson has taught an apparatus as claimed in claim 6, wherein said pointer is a program counter value pointing to a memory address of a memory location storing an instruction of said second instruction set currently being translated (see Col.7 lines 38-50).

22. Regarding claim 11, Robinson has taught an apparatus as claimed in claim 1, wherein said input variables include system state variables not specified within said second instruction (see Col.7 lines 15-21). Here, translated Y instructions specify temporary variables and storage locations prior to updating the state variables and storage locations specified by the non-translated X instructions.

23. Regarding claim 12, Robinson has taught an apparatus as claimed in claim 1, wherein said processor has a register bank (97 of Fig.4) containing a plurality of registers and instructions of said first instruction set execute operations upon register operands held in said registers (see Col.7 lines 25-37).

24. Regarding claim 16, Robinson has taught a method of processing data, said method comprising the steps of:

a. Executing operations as specified by instructions of a first instruction set (see Col.5 lines 51-55).

b. Translating instructions of a second instruction set into translator output signals corresponding to instructions of said first instruction set (see Col.6 lines 20-43), at least one instruction of said second instructions et specifying an operation to be executed using one or more input variables (see Col.6 lines 52-57),

c. In response to an interrupt signal, interrupting execution of operations corresponding to instructions of said first instruction set after completion of execution of a currently executing operation (see Col.7 line 61 – Col.8 line 2),

d. Restarting execution after said interrupt (see Col.7 lines 38-60),

e. Wherein said step of translating generates a sequence of one or more sets of translator output signals corresponding to instructions of said first instruction set to represent said at least one instruction of said second instruction set (see Col.7 lines 6-37), each sequence being such that no changes is made to said one or more input variables until a final operation within said sequence is executed (see Col.11 lines 58-65),

f. After occurrence of an interrupt during execution of a sequence of operations representing said at least one instruction of said second instruction set:

I. If said interrupt occurred prior to starting execution of a final operation in said sequence, then restarting execution at a first operation in said sequence (see Col.7 lines 38-60),

II. If said interrupt occurred after starting execution of a final operation in said sequence, then restarting execution at a next instruction following said sequence (see Col.7 line 61 – Col.8 line 33).

25. Regarding claim 17, Robinson has taught a computer program product holding a computer program for controlling a computer to perform the method of claim 16 (see Col.5 lines 43-50).

***Claim Rejections - 35 USC § 103***

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claims 8-10 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson et al., U.S. Patent No. 5,307,504 as applied to claims 1 and 12 above, and further in view of Dickol et al., U.S. Patent No. 5,898,885.

28. Regarding claim 8, Robinson has taught an apparatus as claimed in claim 1, but has not explicitly taught wherein instructions of said second instruction set specify operations to be executed upon stack operands held in a stack and said input variables include input stack operands.

29. However, Dickol has taught non-native Java instructions that specify operations to be executed on operands held in a stack (see Dickol, Col.4 lines 42-61), and those instruction's corresponding translation into RISC-type native instructions so that redundant execution steps are eliminated and native code execution performance is improved (see Dickol, Col.2 lines 17-39). Because Robinson has taught an apparatus translating instructions from a non-native to a native instruction set (see Robinson, Col.5 lines 43-67), but hasn't explicitly specified if the instructions of the non-native instruction set specify operations to be executed on stack operands, one of ordinary skill in the art would have found it obvious to modify the translation apparatus of Robinson to instead translate instructions specifying operations to be performed on stack

operands in a non-native second instruction set into a native first instruction set in a manner so that redundant execution steps are eliminated, thereby improving processor performance.

30. Regarding claim 9, Robinson in view of Dickol has taught an apparatus as claimed in claim 8, wherein any updating of the state (memory or registers) is not performed until after execution of said final operation has commenced in order to preserve instruction granularity (see Robinson, Col.7 line 38 - Col.8 line 34), but has not explicitly taught wherein the updating of the state includes removing stack operands from the stack.

31. However, Dickol has taught non-native Java instructions that specify operations to be executed on operands held in a stack (see Dickol, Col.4 lines 42-61), and the corresponding translation of those instructions into RISC-type native instructions so that redundant execution steps are eliminated and native code execution performance is improved (see Dickol, Col.2 lines 17-39). Because Robinson has taught an apparatus translating instructions from a non-native to a native instruction set (see Robinson, Col.5 lines 43-67) where updating of the state does not occur until after execution of a final operation has commenced (see Robinson, Col.7 line 38 - Col.8 line 34), and further because the a push or pop of Dickol is a state update (push/pop operates on the stack and registers), one of ordinary skill in the art would have found it obvious to modify the processor of Robinson to only update the state (i.e. pop registers from the stack) after execution of a final operation has commenced so that non-native to native instruction translation can be executed more efficiently (see Dickol, Col.7 lines 5-16) while maintaining instruction granularity (see Robinson, Col.7 lines 38-60).

32. Regarding claim 10, Robinson has taught an apparatus as claimed in claim 8, wherein any updating of the state (memory or registers) is not performed until after execution of said final

operation has commenced in order to preserve instruction granularity (see Robinson, Col.7 line 38 - Col.8 line 34), but has not explicitly taught wherein the updating of the state includes adding stack operands to the stack.

33. However, Dickol has taught non-native Java instructions that specify operations to be executed on operands held in a stack (see Dickol, Col.4 lines 42-61), and the corresponding translation of those instructions into RISC-type native instructions so that redundant execution steps are eliminated and native code execution performance is improved (see Dickol, Col.2 lines 17-39). Because Robinson has taught an apparatus translating instructions from a non-native to a native instruction set (see Robinson, Col.5 lines 43-67) where updating of the state does not occur until after execution of a final operation has commenced (see Robinson, Col.7 line 38 - Col.8 line 34), and further because the a push or pop of Dickol is a state update (push/pop operates on the stack and registers), one of ordinary skill in the art would have found it obvious to modify the processor of Robinson to only update the state (i.e. push registers onto the stack) after execution of a final operation has commenced so that non-native to native instruction translation can be executed more efficiently (see Dickol, Col.7 lines 5-16) while maintaining instruction granularity (see Robinson, Col.7 lines 38-60).

34. Regarding claim 13, Robinson has taught an apparatus as claimed in claim 12, but has not explicitly taught wherein a set or registers within said register bank hold stack operands from a top portion of said stack.

35. However, Dickol has taught wherein a set of registers in a register file hold operands corresponding to a top portion of a stack (see Dickol, Col.2 lines 59-67). Here, when non-native Java paired push and pop instructions are to be translated into native RISC-type instructions, the

translation stores those stack operands, which are on the "top" of the stack (due to the LIFO nature of stacks), in the register file, so that unnecessary data transfers are eliminated, and processor performance is improved (see Dickol, Col.4 lines 42-61). Because Robinson has taught an apparatus translating instructions from a non-native to a native instruction set (see Robinson, Col.5 lines 43-67) with the instructions able to operate on operands in the register file (see Robinson, Col.7 lines 25-37), but hasn't explicitly specified that the operands in the register file are stack operands, one of ordinary skill in the art would have found it obvious to modify the translation apparatus of Robinson to instead translate instructions specifying operations to be performed on stack operands in a non-native second instruction set into a native first instruction set in a manner such that redundant stack operations have their operands stored in the register file so that redundant execution steps can be eliminated, thereby improving processor performance.

36. Regarding claim 14, Robinson has taught an apparatus as claimed in claim 13, wherein an apparatus translating instructions from a non-native to a native instruction set (see Robinson, Col.5 lines 43-67), where updating of the state does not occur until after execution of a final operation has commenced (see Robinson, Col.7 line 38 - Col.8 line 34), but has not explicitly taught wherein said instruction translator has a plurality of mapping states in which different registers within said set of registers hold respective stack operands from different positions within said stack, said instruction translator being operable to move between mapping states when said final operation is executed so as to update said input variables.

37. However, Dickol has taught mapping of registers to different stack operands with the ability to move between the mappings based on whether there is a push or a pop operation (see Dickol, Col.6 lines 27-40), thus allowing non-native to native instruction translation to be

executed more efficiently (see Dickol, Col.7 lines 5-16). Because a push or pop instruction of Dickol is a non-native instruction (see Dickol, Col.6 lines 27-40), one of ordinary skill in the art would have found it obvious to modify the processor of Robinson to map registers of different stack operands with the ability to move between mappings once the final native operation of a non-native push or pop instruction has been executed so that non-native to native instruction translation can be executed more efficiently (see Dickol, Col.7 lines 5-16) while maintaining instruction granularity (see Robinson, Col.7 lines 38-60).

38. Regarding claim 15, Robinson has taught an apparatus as claimed in claim 1, but has not explicitly taught wherein said instructions of said second instruction set are Java Virtual Machine instructions.

39. However, Dickol has taught non-native Java Virtual Machine instructions being translated into RISC-type native instructions (see Dickol, Col.3 lines 49-57) so that redundant execution steps are eliminated and native code execution performance is improved (see Dickol, Col.2 lines 17-39). Because Robinson has taught an apparatus translating instructions from a non-native to a native instruction set (see Robinson, Col.5 lines 43-67), but hasn't explicitly specified the type of non-native instructions, one of ordinary skill in the art would have found it obvious to modify the translation apparatus of Robinson to instead translate Java Virtual Machine instructions into a native first instruction set in a manner so that redundant execution steps are eliminated, thereby improving processor performance.

***Conclusion***

40. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the

patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

41. Patel et al., U.S. Patent No. 6,332,215, has taught a Java hardware accelerator that translates Java bytecode instructions into native CPU instructions.

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

43. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
6/25/2004

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